BIRDS-RPM SATELLITE On-board Computer Command and Data Handling Interface Control Document

Topic:	On Board Computer Interface Control Document
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Version History		
Change Log		
Version	**Date**	**Comments**
1	12/11/2024	Draft inherited from Leopard
2	12/12/2024	Addition of mechanical interfaces
3	15/01/2025	Reworked content of draft Added introduction Added general description Added operational scenario Added system requirements Added non-functional attributes Added performance requirements Added interface requirements Added schedule Added BOM Added appendix
4	14/07/2025	Updated software interface for TUM Added software requirements for Mission Boss Updated mechanical interface section Updated 50 pin assignment table from image to table
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		Realigned section numbers
13	23/01/2026	Updated Appendix A – changed power lines 3v3 to 5v
14	25/01/2026	Updated Appendix A – removed new trx ocp, changed dio ito one way

Table of Contents

1 Introduction

The purpose of this document is to define and document the BIRDS-RPM's On-Board Computer (OBC) Command and Data Handling (CDH) subsystem functionality, processes, constraints, and interfaces with other subsystems to ensure compatibility and clarity.

1.1 Overview

The OBC-CDH is a system of software and hardware connections that enable the collection and storage of the satellite's health telemetry data and mission specific payload data The OBC-CDH is being developed with C, identical in non-mission specific operation scenario to the previous satellites developed in the BIRDS series but different in software implementation as it inherits base code and hardware from the Kyutech Kitsune line of satellites.

1.2 Scope of this Document

This document describes the interfaces between the OBC-CDH - built primarily on the OBC/EPS Printed Circuit Board (PCB) - subsystem components and the other subsystems of BIRDS-RPM satellite's main bus and mission payloads. These interfaces include the mechanical, electrical, data, and operational interfaces.

The constraints of the system are also detailed.

I

Interface Requirements

2 Interfaces

The purpose of this section is to describe the mechanical, electrical, data, and thermal interfaces between the OBC-CDH subsystem and other satellite subsystems.

2.1 Block Diagram for OBC-CDH

The OBC/EPS assembly employs four primary microcontrollers: **MAIN PIC** (PIC18F67J94 - command scheduling and execution), **COM PIC** (PIC18F67J94 - interface to UHF transceivers and ground link), **RESET PIC** (PIC18F67J94 - power line control and system resets), and **Mission Boss PIC** (power DIO switching for mission boards). A **START PIC** (PIC16F1789) provides redundancy for the RESET PIC and initiates power-up if the RESET PIC is unavailable. The MAIN PIC issues commands to the Mission Boss and mission boards via the **CPLD**. The Mission Boss and CPLD reside on the **backplane board** (external to the OBC/EPS board).

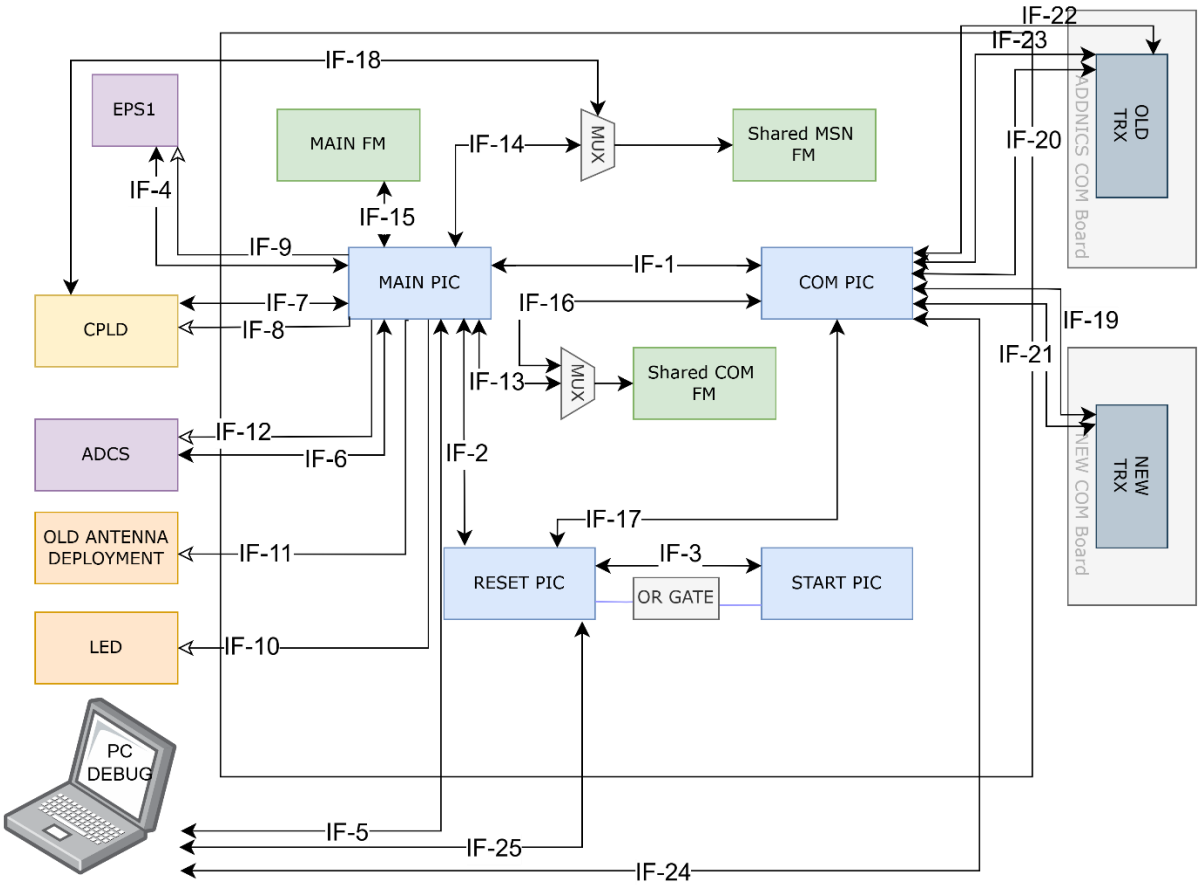


*Figure **Error! Use the Home tab to apply 0 to the text that you want to appear here.**-1 OBC/EPS Board Interface Diagram*

2.1.1 Interface Inventory

Table 3-1 OBC/EPS Board Interface Table

IF ID	Endpoints	Direction	Data Interface	Key Parameters
IF-1	Main PIC ↔ COM PIC	Bi-directional	UART	baudrate=115200, 8-N-1, CRC16
IF-2	Main PIC ↔ Reset PIC	Bi-directional	UART	baudrate=19200, 8-N-1, CRC16
IF-3	Reset PIC ↔Start PIC	Bi-directional	UART	baudrate=19200, 8-N-1, CRC16

IF-4	Main PIC ↔ EPS1	Bi-directional	UART	baudrate=115200, 8-N-1, CRC16
IF-5	Main PIC ↔ PC	Bi-directional	UART	baudrate=57600, 8-N-1, CRC16, debugging
IF-6	Main PIC ↔ADCS PIC	Bi-directional	UART	baudrate=115200, 8-N-1, CRC16,
IF-7	Main PIC ↔ CPLD	Bi-directional	UART	baudrate=115200, 8-N-1, CRC16, ACK/NACK, data from missions
IF-8	Main PIC → CPLD	OBC→CPLD	DIO(3)	CPLD power enable, 3 DIO pins
IF-9	Main PIC → EPS1	OBC→EPS Kill	DIO	Kill switch
IF-10	Main PIC → LED	OBC→LED	DIO	Switch 3ms from inhibit removal
IF-11	Main PIC → Antenna Deployment	OBC→ Burner Circuit	DIO	FIRE pulse=40mins from inhibit removal
IF-12	Main PIC → ADCS	OBC→ADCS	DIO	ADCS Board power enable
IF-13	Main PIC ↔ COMFM	Bi-directional	SPI	baudrate=1000000, shared COM flash memory
IF-14	Main PIC ↔ MSNFM	Bi-directional	SPI	baudrate=1000000, shared mission flash memory
IF-15	Main PIC ↔ MainFM	Bi-directional	SPI	baudrate=1000000, main flash memory
IF-16	COM PIC ↔ COMFM	Bi-directional	SPI	baudrate=1000000, shared COM flash memory
IF-17	COM PIC ↔ Reset PIC	Bi-directional	UART	baudrate=115200, 8-N-1, CRC16
IF-18	CPLD ↔ MSNFM	Bi-directional	SPI	baudrate=1000000, mission access to shared mission flash memory
IF-19	COM PIC ↔ NewTRX	Bi-directional	UART	baudrate=115200, 8-N-1, CRC16
IF-20	COM PIC ↔ OldTRX	Bi-directional	UART	baudrate=115200, 8-N-1, CRC16
IF-21	COM PIC → NewTRX	OBC→ NewTRX	DIO	Enable DIO
IF-22	COM PIC → OldTRX	OBC→ OldTRX	DIO(2)	2 analog DIO
IF-23	COM PIC → OldTRX	OBC→ OldTRX	DIO(3)	3 digital DIO
IF-24	COM PIC ↔ PC	Bi-directional	UART	baudrate=57600, 8-N-1, CRC16, debugging
IF-25	RESET PIC ↔ PC	Bi-directional	UART	baudrate=9600, 8-N-1, CRC16, debugging

2.1.2 Internal Interconnect Matrix

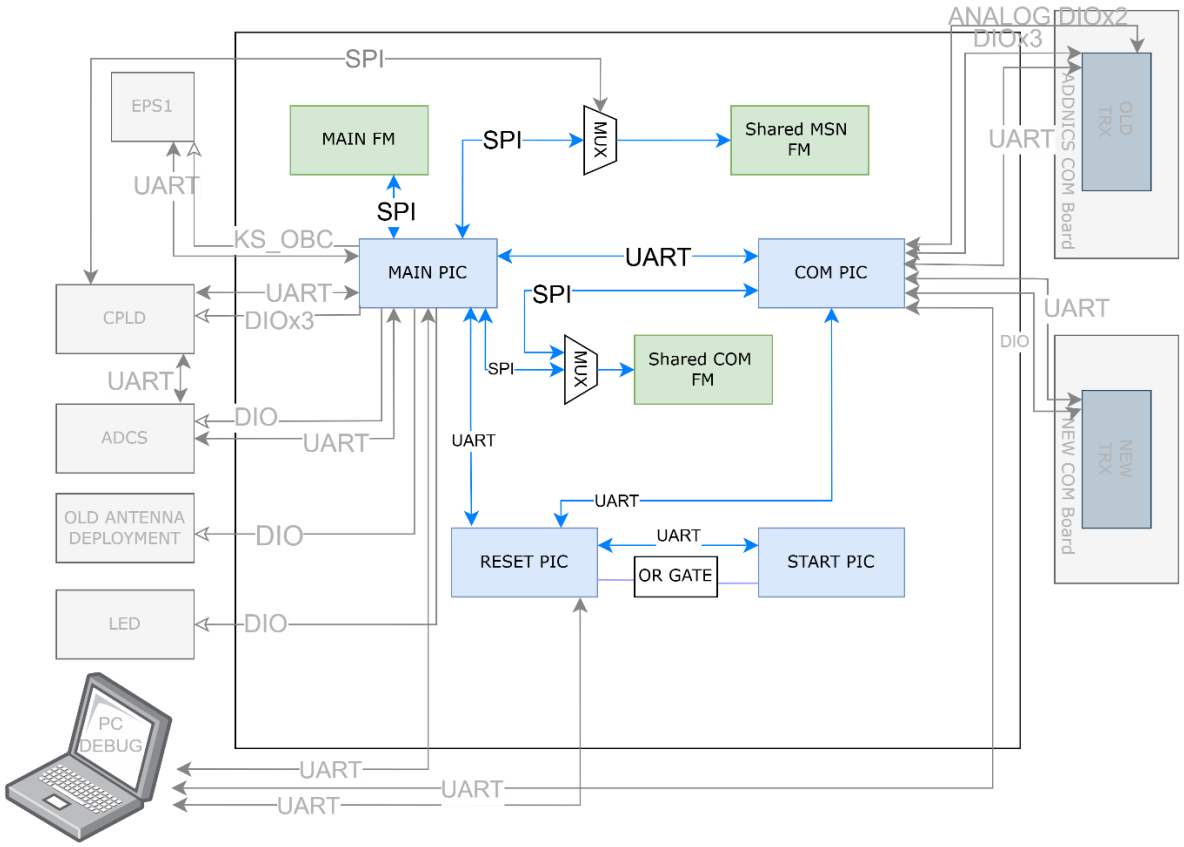


Figure 3-2 Internal MCU relations in OBC-EPS Board

The full MCU level internal pin assignment for all MCUs on the OBC/EPS board can be found in this file inside the corresponding sheets; MAIN, COM, RESET, START.

2.2 Mechanical interfaces

2.2.1 Connector type & pinning

The OBC board mates to the backplane using one 50-pin and two 4-pin board-to-board connectors, polarized and keyed.

Nominal connector family: Hirose A3C series (A3C-50DA-2DSA(71) for 50-pin and A3C-4DA-2DSA(71) for 4-pin).

Backward compatibility: the 50-pin connector is backward-compatible with the original 50-pin backplane footprint.

Number of rows (mating part): 2
Mounting pitch: 2.0 mm
Opening Pitch :2.0 mm
Body length (pitch direction) :50.0 mm
Body width (depth): 4.0 mm
Body height: 4.2 mm
Board mounting method: Through-hole DIP
PCB Mounting Style: Standard Onboard
Board fixing method: soldering

Mating orientation: silkscreen white dot on pin 1 on the boards pin-1 at board corner (see Table 3-1 for pin map).

Operating temperature range Max.: 85°C
Operating temperature range Min.: -55°C

Data obtained from official datasheet at this URL.

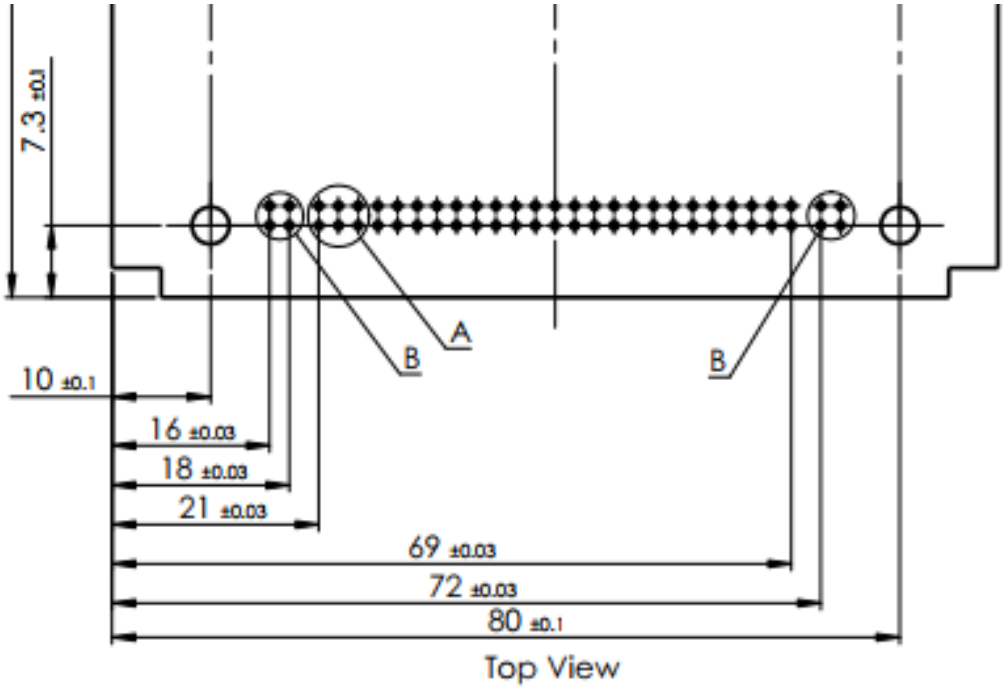


Figure 3-3 OBC/EPS Board 50pin connector 2D Drawing

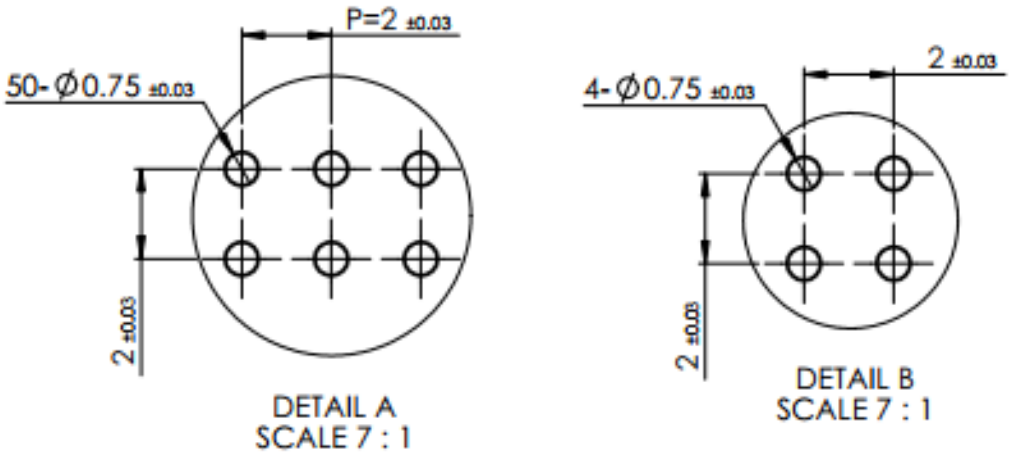


Figure 3-4 OBC/EPS Board 50pin connector Detailed 2D Drawing

The full 2D drawing can be found in Appendix B.

Figure 3-5 Image of OBC/EPS Board 50pin connector

2.2.2 OBC/EPS Board CAD

The OBC-EPS Board shall be manufactured in accordance with the following specifications (units in mm):

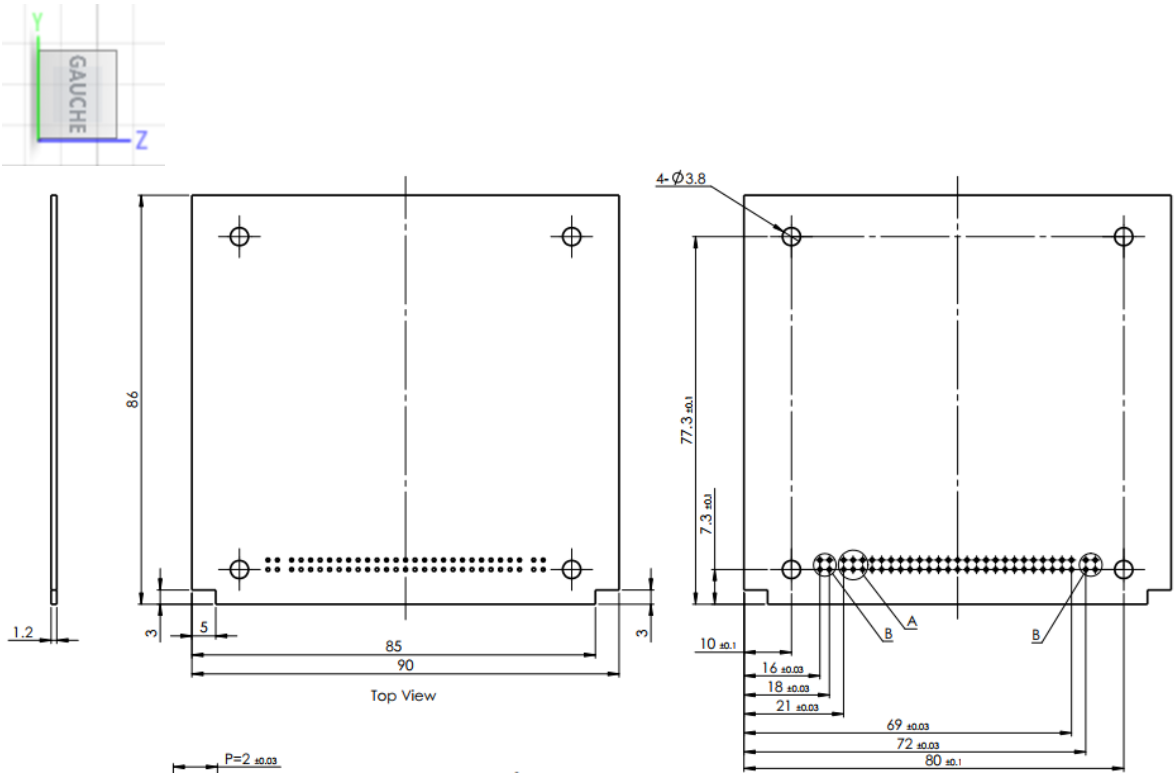


Figure 3-6 OBC/EPS Board 2D Drawing

The full 2D drawing can be found in Appendix B.

Figure 3-7 Image of OBC/EPS Board Front

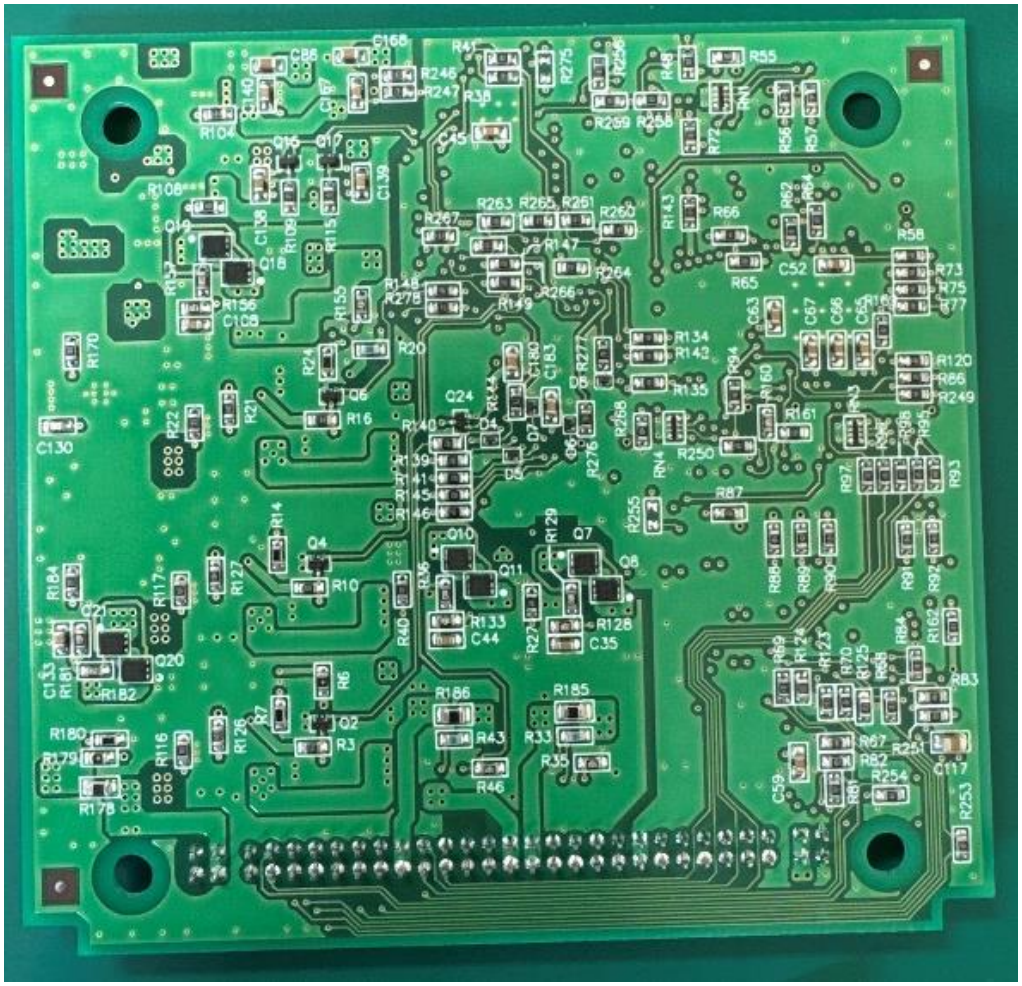


Figure 3-8 Image of OBC/EPS Board Back

2.3 Electrical interfaces

This section defines the OBC/EPS Board electrical interfaces, including power rails, limits, protections, grounding, and connector pin assignments. Nominal voltage and current requirements can be found in the EPS ICD. Unless stated otherwise, logic levels are 3.3 V CMOS, polarity is as marked on the pin maps, and all rails include brown-out/POR constraints defined by the EPS. Detailed assignments for the 50-pin backplane connector are provided in Table 3-2. Full pin map with pin voltages and baud rates can be found in this file inside the 'BIRDSRPM OBCEPS 50-PIN' sheet.

2.3.1 50-Pin Connector Map (Backplane Integration)

Table 3-2 50-pin connector map

Signal Name (Left)	Pin Number	Pin Number	Signal Name (Right)
GND_SYS	1	2	GND_SYS
SUP_UNREG_3	3	4	SUP_UNREG_3
DEV1 PGC	1	2	DEV2 PGD
OBC_DIO1	3	4	DEV4 MCLR_RP

DEV5 MCLR_CP	5	6	DEV6 MCLR_MP
UART_TRX-CP	7	8	UART_CP-TRX
CPLD_CTRL1	9	10	CPLD_CTRL2
CPLD_CTRL3	11	12	DEV12_MCLR_SP
GND SYS	13	14	GND SYS
SUP_5V0_1	15	16	SUP_5V0_1
UART_MP-DBG	17	18	UART_DBG-MP
UART_MP-EPS1	19	20	UART_EPS1-MP
OBC_DIO2	21	22	OBC_DIO3
SUP UNREG 1	23	24	SUP UNREG 1
SUP_5V0_2	25	26	SUP_5V0_2
UART MP-CPLD	27	28	UART CPLD-MP
Raw_Power	29	30	Raw_Power
SPI_CSn_CPLD-FM	31	32	SPI_SDO_CPLD2FM
SPI_SDI_FM-CPLD	33	34	SPI_SCK_CPLD2FM
SUP_UNREG_2	35	36	SUP_UNREG_2
OBC_DIO0	37	38	UNASSIGNED
Kill_OBC	39	40	UART_CP-NTRX
UART_NTRX-CP	41	42	UNASSIGNED
DIO0 (CP-NTRX)	43	44	DIO1 (CP-TRX_ONOFF)
DIO2 (CP-TRX_CW)	45	46	DIO3 (CP2TRX_CWKEY)
ANALOG DIO4 (TRX_TEMP)	47	48	ANALOG DIO5 (TRX_RSSI)
SUP_3V3 1	49	50	SUP_3V3 1
SUP_12V	1	2	SUP_12V
RAW_POWER	3	4	RAW_POWER

2.4 Communications Interfaces

Two UHF communications options are supported:

- Legacy transceiver (Addnics UHF) — flight heritage from early BIRDS series.
- In-house UHF transceiver — lower-cost board targeted for space qualification in this mission.

Both are interfaced by the COM PIC; validated uplink commands are forwarded to the MAIN PIC. Downlink telemetry/CW frames are generated by MAIN and passed to COM for RF transmission.

UART settings (unless otherwise specified): 8-N-1, logic levels 3.3 V CMOS.

2.4.1 Uplink Command Format

Table 3-3 Uplink Command Format Table

Header	Sat ID	Command Format	Command ID	Reservation Time	Mission Command Data							CRC	

Header (1 byte): Leading byte for the command signal. Set by the GS Software.
Satellite ID (1 byte): It is a unique value designated for each satellite.
Command Format (1 byte): Determines which PIC the command is designated (0xA0 - MAIN PIC, any - COM PIC, 0x33 - RESET PIC, etc.).
Command ID (1 byte): Determines which command to execute. The upper 4 bits describe which mission MCU the command is for the lower 4 bits describe what command to execute.
Reservation Time (1 byte): Designates the reservation time for a specific mission. Delays command execution by the specified time.
Command Data (7 bytes): Describes the command data to be included in the command.
CRC (2 bytes): Cyclic Redundancy Check for error checking. Set by the GS Software.

2.4.2 UHF Uplink Command Specifications

Command format (Ground Station → Main PIC)

Table 3-4 UHF Uplink Command Data Frame Table

Byte Index	Value / Field	Description
0	0x42	Header
1	0x57	Satellite ID
2	0x00	Reservation Time
3	CMD_ID1	Command ID1
4	CMD_ID2	Command ID2
5–11	Variable Data	Mission payload (0–7B)
12	Checksum 1	CRC16 over bytes 0–11, LSB
13	Checksum 2	CRC16 over bytes 0–11, MSB

Internal command envelope used by the MAIN PIC when dispatching to mission MCUs and subsystems is specified within the corresponding subsystem software ICD.

Non-Volatile Memory

3 Non-Volatile Memory Map

Addresses This section defines the logical allocation of SPI NOR flash used by OBC-CDH for flags, logs, telemetry, and mission data. Allocations are aligned to device sector = 64 KB and sub-sector/page = 4 KB. All regions are exclusive, non-overlapping, and reserved for the stated purpose.

Table 4-1 Non-Volatile Memory Map Table

Region	Sector Start	Sector End	Start Addr (hex)	End Addr (hex)	# Units	Size (KB)	Size (MB)
BOOT_FLAGS	0	0	0x00000000	0x00001000	1 page	4	0.0039
OBC_FLAGS	0	0	0x00001000	0x00002000	1 page	4	0.0039
ADDR_FLAGS	0	0	0x00002000	0x00003000	1 page	4	0.0039
SCHEDULED_CMD	0	0	0x00003000	0x00004000	1 page	4	0.0039
FLAGS TOTAL	0	0	0x00000000	0x00004000	4 pages	16	0.0156

FLASH_LOG	1	16	0x00010000	0x00110000	16 sectors	1,024	1.000
FLASH_TELEMETRY	17	748	0x00110000	0x02ED0000	732 sectors	46,848	45.750
FLASH_CCB	749	1004	0x02ED0000	0x03ED0000	256 sectors	16,384	16.000
FLASH_APRS	1005	1132	0x03ED0000	0x046D0000	128 sectors	8,192	8.000
FLASH_RAD_LOG	1133	1133	0x046D0000	0x046E0000	1 sector	64	0.0625
FLASH_RAD	1134	1260	0x046E0000	0x04ED0000	127 sectors	8,128	7.9375
FLASH_EOBC	1261	1516	0x04ED0000	0x05ED0000	256 sectors	16,384	16.000
FLASH_ADCS_HS	1517	1523	0x05ED0000	0x05F40000	7 sectors	448	0.4375
FLASH_ADCS_GPS	1524	1528	0x05F40000	0x05F90000	5 sectors	320	0.3125
FLASH_ADCS_TELEMETRY	1529	1784	0x05F90000	0x06F90000	256 sectors	16,384	16.000

3.1 Flash memory summary

Device capacity: 128 MB = 131,072 KB
Allocated (from table): 114,192 KB ≈ 111.6 MB
Headroom (free): 16,880 KB ≈ 16.48 MB
Breakdown used in the sum:
FLAGS(16) + LOG(1,024) + TELEMETRY(46,848) + CCB(16,384) + APRS(8,192) + RAD_LOG(64) + RAD(8,128) + EOBC(16,384) + ADCS_HS(448) + ADCS_GPS(320) + ADCS_TLM(16,384) = 114,192 KB
Alignment: All region start/end addresses are sector-aligned (multiples of 0x10000 for 64 KB sectors), enabling clean erase/protect per partition.

3.2 Flash parameters

MEMORY_SIZE = 128 * 1024 * 1024 = 134,217,728 bytes = 131,072 KB
MEMORY_SECTOR_SIZE = 64 * 1024 = 65,536 bytes = 64 KB
MEMORY_SUBSECTOR_SIZE = 32 * 1024 = 32,768 bytes = 32 KB
MEMORY_PAGE_SIZE = 4 * 1024 = 4,096 bytes = 4 KB
Addressing rule (sector-aligned regions):
address = sector_number × 0x10000

Examples (sector-aligned):
FLASH_LOG_START = 1 × 0x10000 = 0x0001_0000
FLASH_TELEMETRY_START = 17 × 0x10000 = 0x0011_0000
(…and so on for each region)

4 Subsystem Requirements Sheets

4.1 Bus

4.1.1 PC Debug

To view the debug information from Main PIC on a computer terminal, the communication interface is a 3.3V TTL UART configured with the following parameters: **baud rate** of 57600 bps, **data bits**: 8, **stop bits**: 1, **parity**: none, and **flow control**: none.

MAIN PIC to PC Debug UART Interface overview

- Voltage level: 3.3V TTL
- Baud rate 57600 bps,
- Data bits: 8,
- Stop bits: 1,
- Parity: None,
- Flow control: None

4.1.2 MISSION BOSS

Main PIC communicates with Mission Boss PIC by UART via the Complex Programmable Logic Device (CPLD) situated on the backplane board. The communication interface is a 3.3V TTL UART configured with the following parameters: **baud rate** of 115200 bps, **data bits**: 8, **stop bits**: 1, **parity**: none, and **flow control**: none.

UART Interface overview

- Voltage level: 3.3V TTL
- Baud rate 115200 bps,
- Data bits: 8,
- Stop bits: 1,
- Parity: None,
- Flow control: None

4.1.3 COM

Main PIC communicates with COM PIC by UART via the CPLD. The communication interface is a 3.3V TTL UART configured with the following parameters: **baud rate** of 115200 bps, **data bits**: 8, **stop bits**: 1, **parity**: none, and **flow control**: none. COM PIC communicates with Reset PIC Another data transfer interface is implemented via SPI to the shared COM flash memory, where the COM PIC operates as the SPI master and the flash memory is the slave. Additional details can be found in the COM ICD here.

Table 5-1 COM PIC Interface Table

Interface parameter	**COM ↔ MAIN UART**	**COM ↔ RESET UART**	**COM ↔ PC UART**	**COM SFM SPI**
Voltage level	3.3V TTL	3.3V TTL	3.3V TTL	3.3V
Baud rate (bps)	115200	38400	57600	1000000
Data bits	8	8	8	8
Stop bits	1	1	1	-
Parity	None	None	None	-
Flow control	None	None	None	-

4.1.4 EPS

Main PIC communicates to EPS PIC located on the EPS1 board by UART. The communication interface is a 3.3V TTL UART configured with the following parameters: **baud rate** of 115200 bps,

data bits: 8, **stop bits**: 1, **parity**: none, and **flow control**: none. Additionally, a DIO interface that operates the OBC Kill Switch trigger in the EPS PIC is controlled by Main PIC. Additional details can be found in the EPS ICD here.

UART Interface overview

- Voltage level: 3.3V TTL
- Baud rate 115200 bps,
- Data bits: 8,
- Stop bits: 1,
- Parity: None,
- Flow control: None

4.1.5 RESET

Main PIC communicates to Reset PIC by UART. The communication interface is a 3.3V TTL UART configured with the following parameters: **baud rate** of 115200 bps, **data bits**: 8, **stop bits**: 1, **parity**: none, and **flow control**: none.

Table 5-2 Reset PIC Interface Table

Interface parameter	**RESET ↔ MAIN UART**	**RESET ↔ COM UART**	**RESET ↔ PC UART**	**RESET ↔ START UART**
Voltage level	3.3V TTL	3.3V TTL	3.3V TTL	3.3V
Baud rate (bps)	19200	19200	57600	19200
Data bits	8	8	8	8
Stop bits	1	1	1	1
Parity	None	None	None	None
Flow control	None	None	None	None

4.1.6 START

Start PIC communicates with Reset PIC by UART. The communication interface is a 3.3V TTL UART configured with the following parameters: **baud rate** of 19200 bps, **data bits**: 8, **stop bits**: 1, **parity**: none, and **flow control**: none.

UART Interface overview

- Voltage level: 3.3V TTL
- Baud rate 115200 bps,
- Data bits: 8,
- Stop bits: 1,
- Parity: None,
- Flow control: None

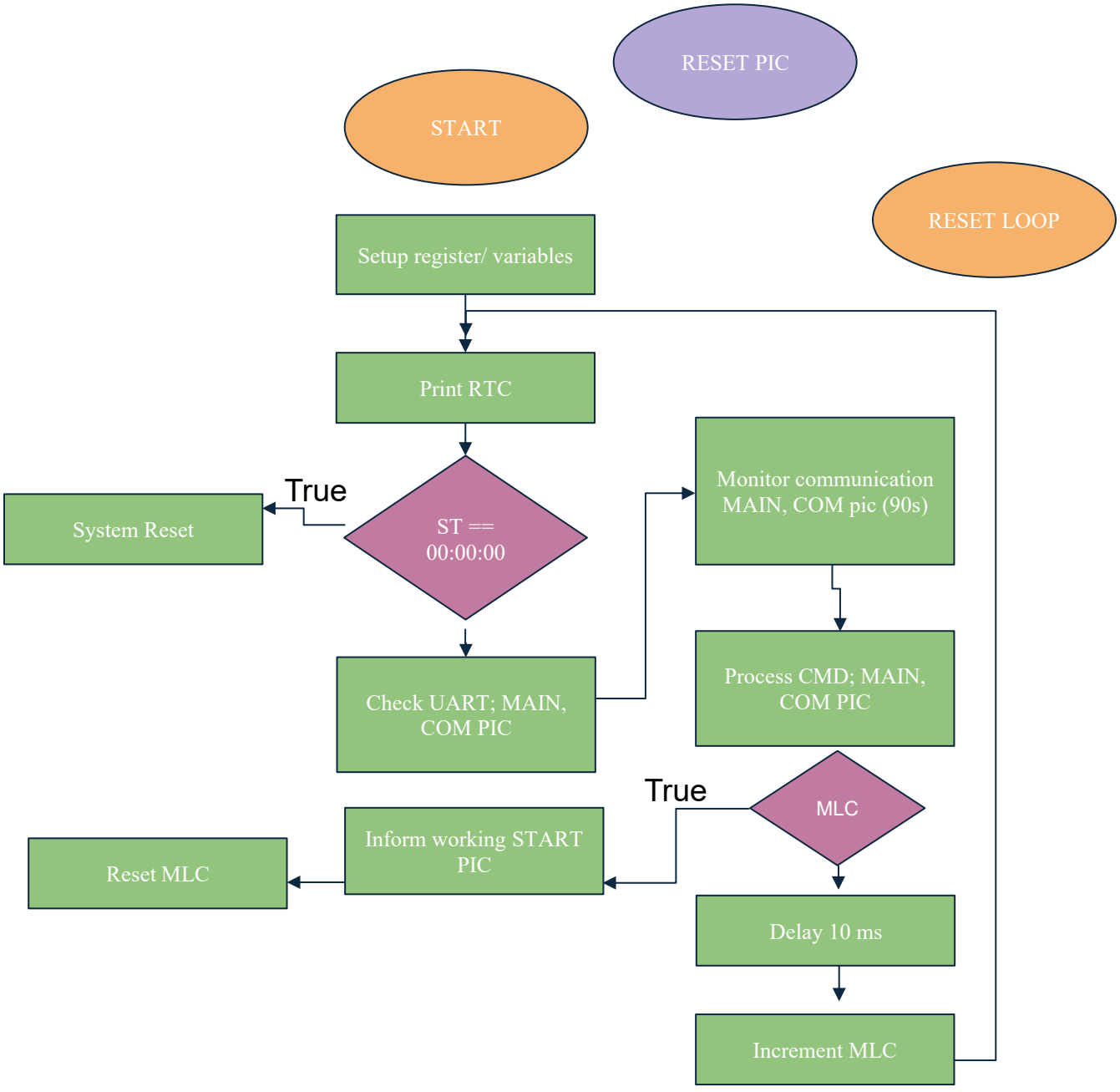
4.2 Payloads

The interfaces between the OBC-CDH and mission boards are specified in individual software interface documents.
The software ICD of ADCS can be found here.
The software ICD of TUM can be found here.
The software ICD of OSIL can be found here.
The software ICD of CABUREI can be found here.

5 Operation Scenarios

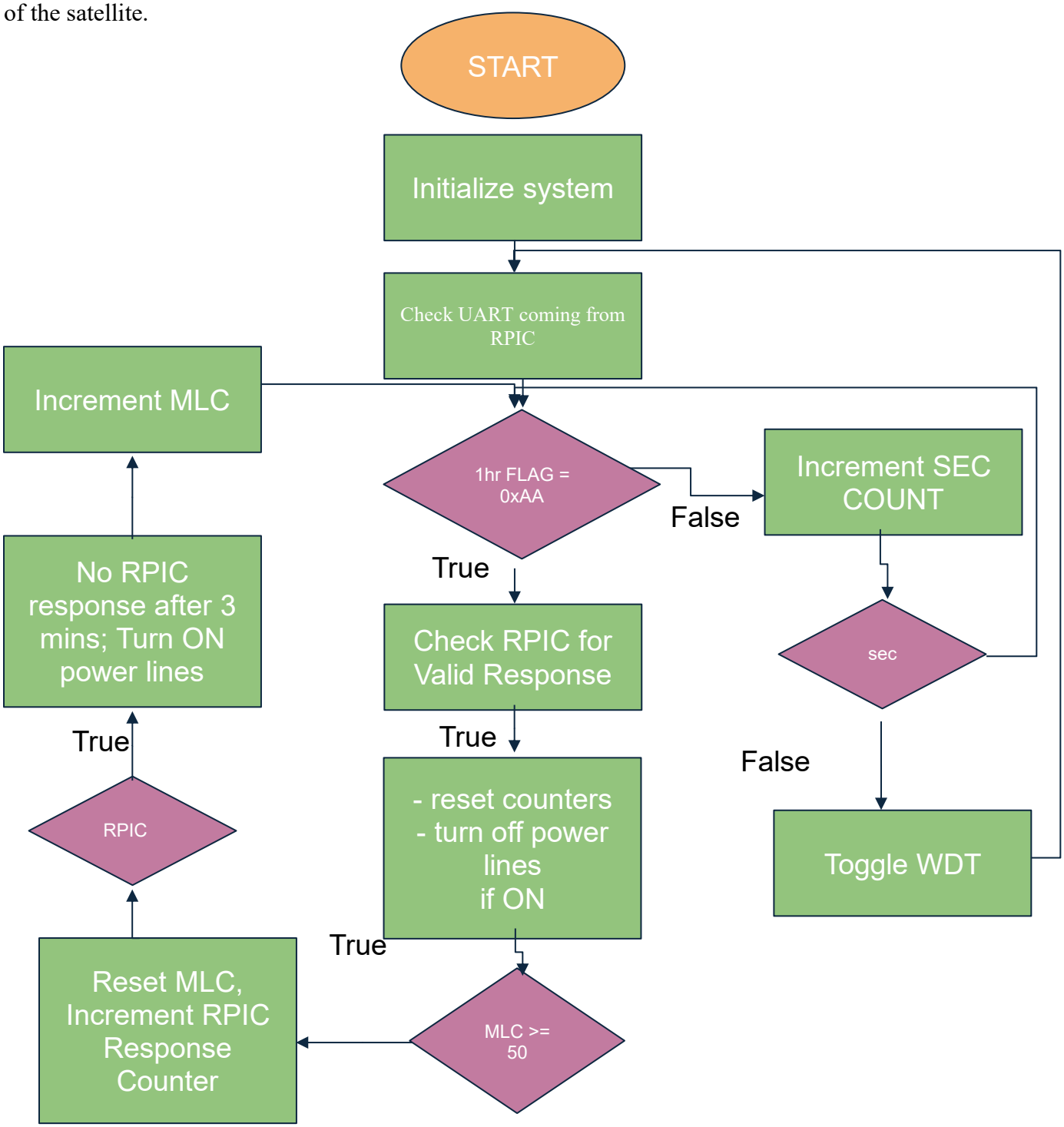
5.1 Scenario A: Reset PIC

This section describes the operation scenario of the Reset PIC starting from the launch of the satellite.



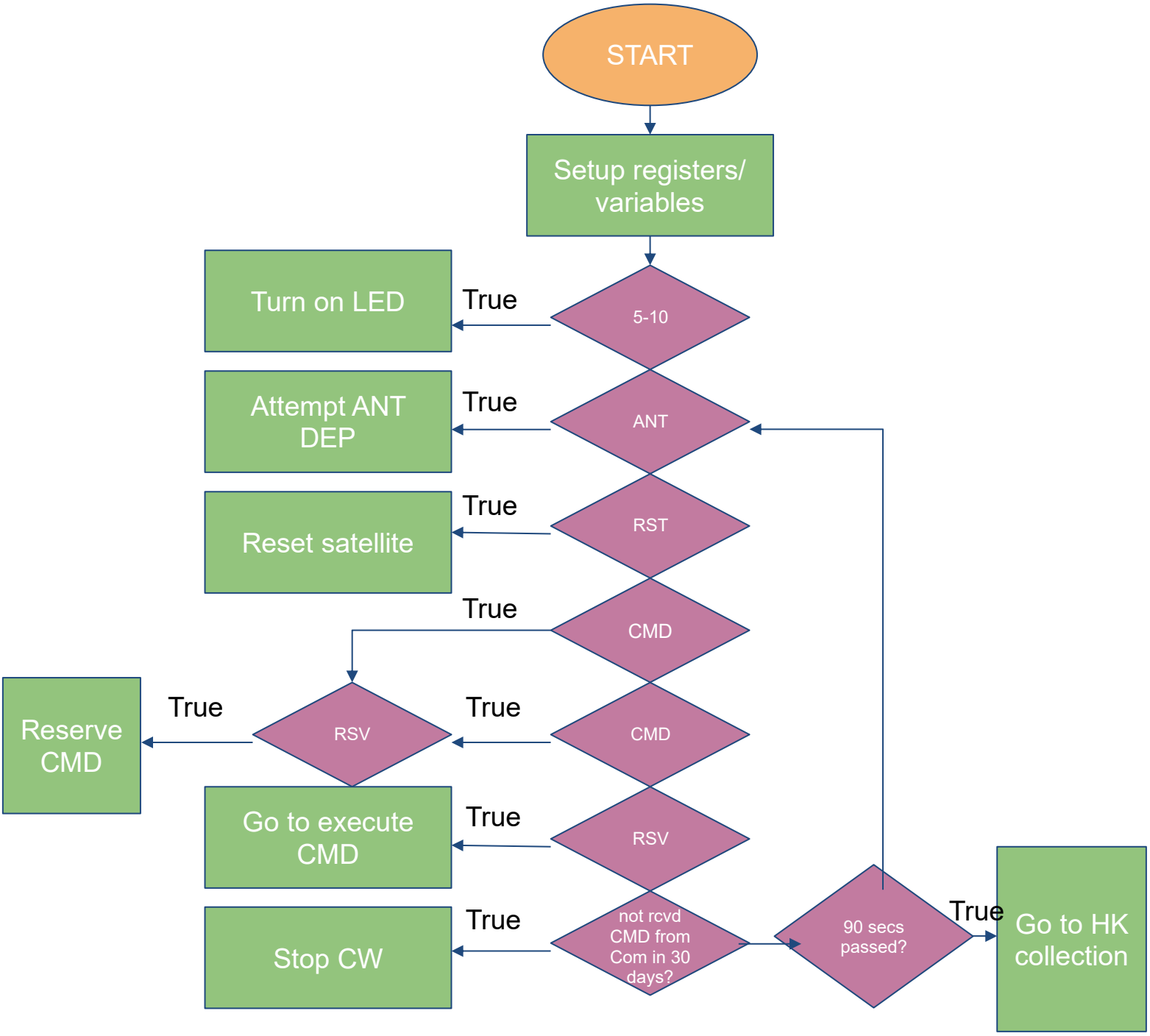
5.2 Scenario B: Start PIC

This section describes the operation scenario of the Start PIC starting from the launch of the satellite.



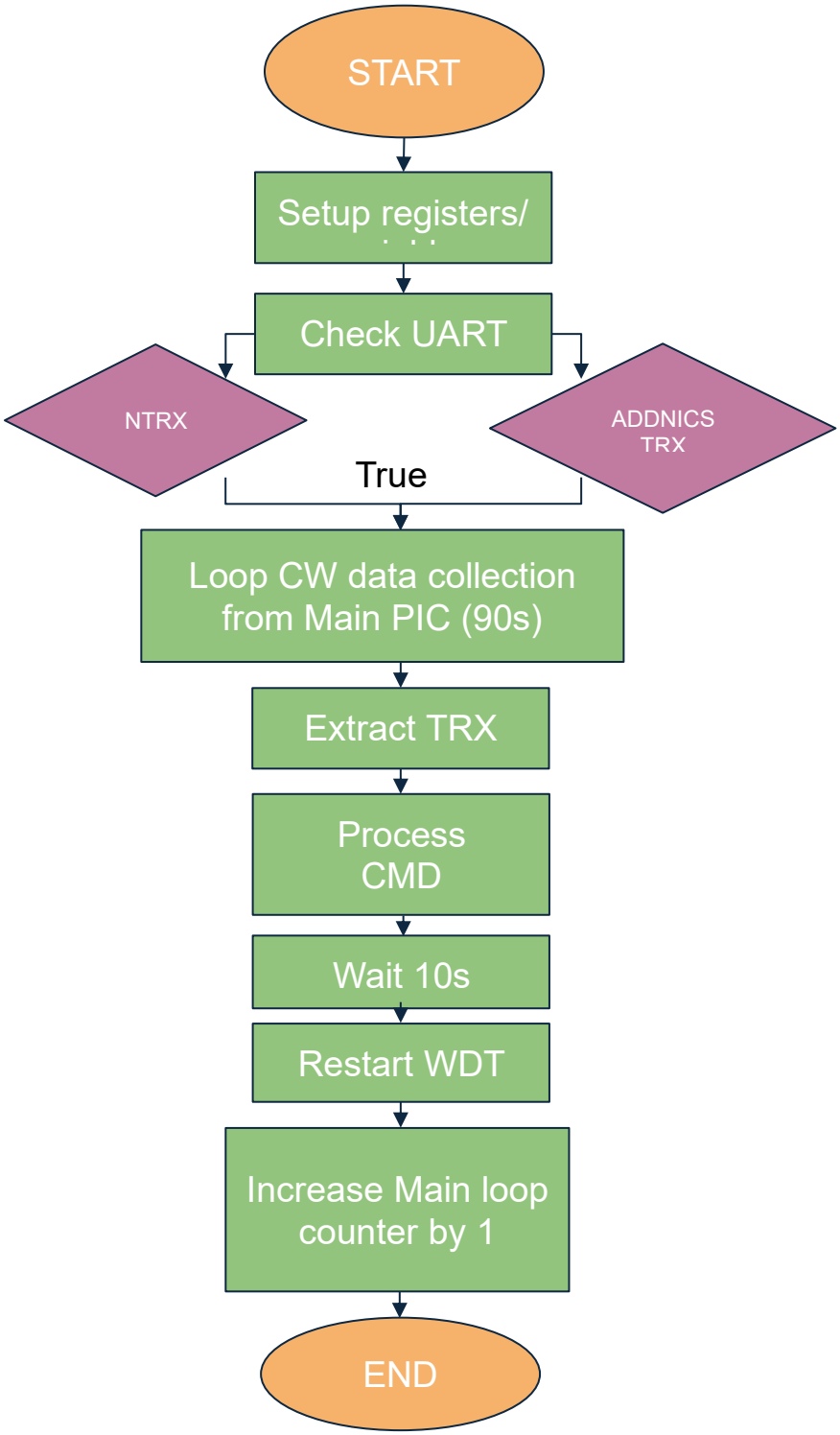
5.3 Scenario C: Main PIC

This section describes the operation scenario of the Main PIC starting from the launch of the satellite.



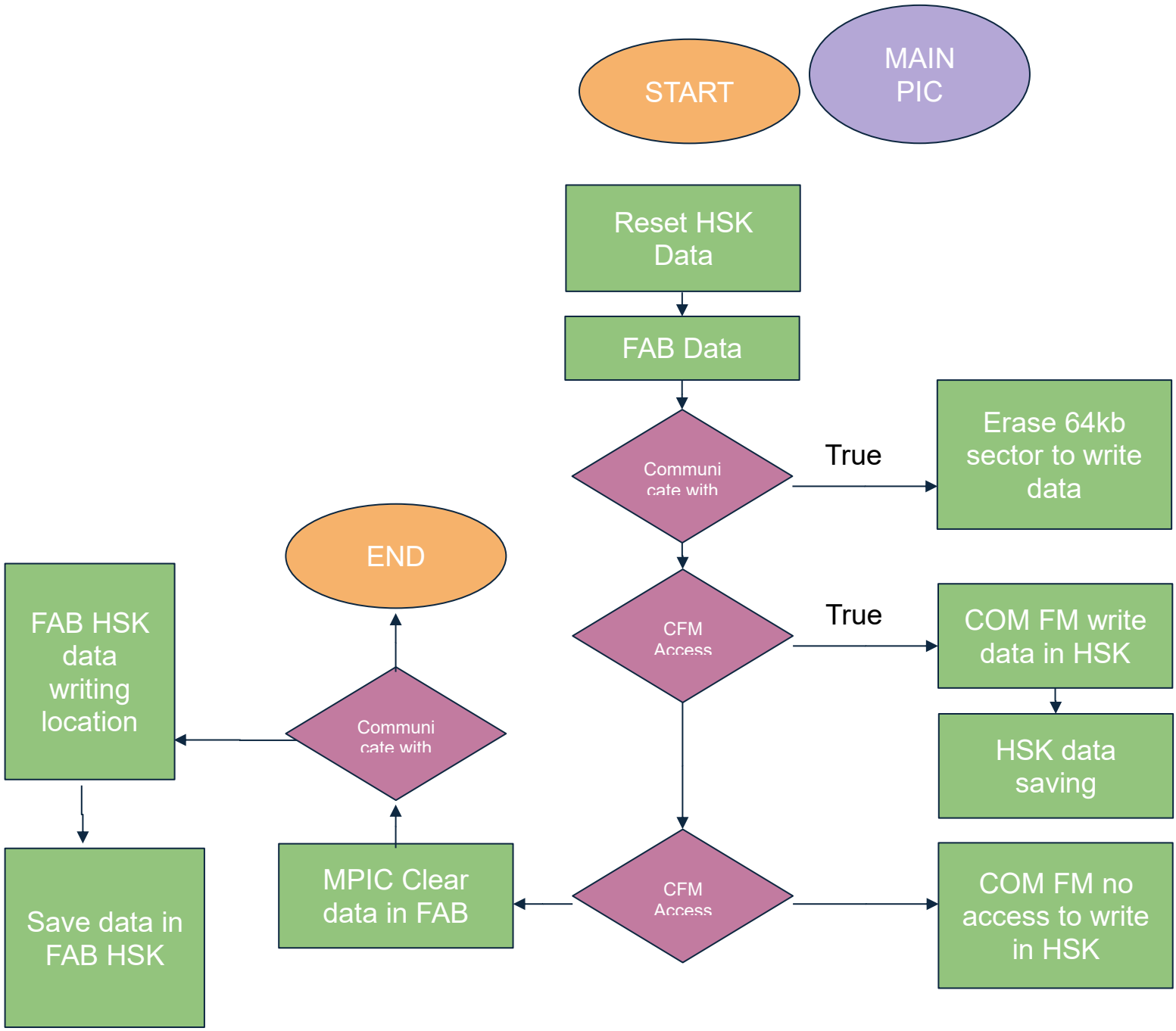
5.4 Scenario D: Com PIC

This section describes the operation scenario of the Com PIC starting from the launch of the satellite.



5.5 Scenario E: HK Collection

This section describes the operation scenario of the Main PIC relates with FAB PIC, Reset PIC for housekeeping starting from the launch of the satellite.



6 Cyclic Redundancy Check (CRC) Implementation

In the BIRDS-RPM satellite, a CRC calculation code is used to verify packet integrity and confirm that the uplink command format is valid. This is through a 16-bit checksum at the end of the command formats. The checksum is a standard **16-bit CRC-16-CCITT** value that is transmitted as two separate 8-bit fields.

The CRC is calculated over the packet data (excluding the last 2 bytes which contain the CRC itself) and then compared against the received CRC value to validate the packet.

This implementation follows the standard CRC-16-CCITT algorithm, which provides good error detection capabilities for communication protocols where data integrity is critical.

1. CRC Calculation Code

```
#ifndef CRC16_H
#define CRC16_H

#include <stdint.h>

//! CRC calculation function
uint16_t mk_crc(uint8_t* data, uint8_t size)
{
    uint32_t crcreg = 0xffff;
    uint32_t calc = 0x8408;
    for (uint32_t k = 0; k < size; k++) {
        uint8_t cal_data = data[k];
        for (uint32_t i = 0; i < 8; i++) {
            uint8_t w = (crcreg ^ cal_data) & 0x0001;
            crcreg = crcreg >> 1;
            if (w == 1) {
                crcreg = crcreg ^ calc;
            }
            cal_data = cal_data >> 1;
        }
    }
    crcreg = crcreg ^ 0xffff;
    return crcreg;
}

#endif /* CRC16_H */
```

2. CRC Calculation Method

The `mk_crc` function implements a CRC-16 calculation with the following characteristics:

Key Parameters:
- Initial value: `0xFFFF` (loaded into `crcreg`)
- Polynomial: `0x8408` (stored in `calc`)
- Final XOR: `0xFFFF` (applied at the end)
- Input reflection: No
- Output reflection: No

Polynomial Analysis:
The polynomial `0x8408` in binary is: `1000 0100 0000 1000`

This corresponds to the polynomial: $x^{16} + x^{12} + x^5 + 1$

This is the CRC-16-CCITT (Kermit) polynomial, which is a widely used standard for error detection in communication protocols.

Algorithm Steps:
1. Initialize: Set `crcreg = 0xFFFF`
2. Process each byte: For each byte in the input data
3. Process each bit: For each bit in the current byte (LSB first)
   - XOR the LSB of `crcreg` with the current bit of input data
   - Right-shift `crcreg` by 1
   - If the XOR result was 1, XOR `crcreg` with the polynomial `0x8408`
   - Right-shift the input data by 1
4. Final XOR: XOR the result with `0xFFFF`
5. Return: Return the 16-bit CRC value

Bill of Materials

PART NUMBER	Description	REFERENCE	Quantity	MANUFACTURER I	PART NUMBER
SN74CB3Q3257	4-Bit 1-of-2 FET Multiplexer/Demultiplexer	U33,U35	2		
TPS63020-Q1	Buck-boost converter. Power Supply	U1,U4	2		
3300pF	CAPACITOR	C9,C19,C28,C35,C44,C85, C93	7		
10nF	CAPACITOR	C31	1		
560pF	CAPACITOR	C81,C89	2		
22uF	CAPACITOR	C3,C4,C5,C6,C14,C15,C16, C17,C25,C26,C27,C80,C84, C88,C92	15		
33pF	CAPACITOR	C79,C87	2		
1uF	CAPACITOR	C24	1		
6800pF	CAPACITOR	C98	1		
0.1uF	CAPACITOR	C7,C11,C18,C22,C32,C36, C37,C43,C45,C46,C47,C48, C49,C51,C52,C54,C55,C59,	53		
10uF	CAPACITOR	C1,C2,C8,C10,C12,C13,C20, C21,C23,C29,C30,C33,C34, C40,C41,C62,C82,C83,C90,	22		
12pF	CAPACITOR	C39,C42,C56,C57,C58,C60 C104,C105	8		
PIC18F67J94	COM PIC, MAIN PIC, RESET PIC (64 Pin)	U23,U44,U51	3		
2row-50pin header R/A	Connector	CN302	1		
CONN SOCKET 3x2/SM	Connector	J2,J3,J5,J6	4		
LTC3530EDDTRPBF	DC/DC converter	U36,U39	2		
DTC144EKA	Digital Transistor (Bias Resistor Built-in Transistor)	Q2,Q4,Q6,Q9,Q12,Q15,Q17 Q21	8		
SN74LVC2G34DBVR	Dual Buffer Gate	U12,U20,U27,U28,U29,U46, U50	7		
UMD5N	Dual Digital Transistor (Bias Resistor Built-in Transistor)	U16	1		
SN74CB3Q3305	Dual FET Bus Switch, high-bandwidth FET bus	U19,U25,U41,U52,U56,U57, U58	7		
BAS40-05W	General-purpose dual Schottky diode	D2	1		
TPS61235RWLT	high current, high efficiency synchronous boost converter	U7	1		
2N7002/SOT	High efficiency power management applications	Q19	1		
LT6106	high side current sense amplifier.	U3,U6,U9,U11,U17	5		
4.7uH	INDUCTOR	L4, L5	2		
1.5uH	INDUCTOR	L1,L2	2		
1uH	INDUCTOR	L3	1		
OV-7604-C7	Low Power Clock Oscillator 32.768 kHz, Low Frequency SMD Oscillator	U45	1		
MT25QL01GBBB8ES	Micron Serial NOR Flash Memory 3V, Multiple I/O, 4KB, 32KB, 64KB Sector Erase	U21,U32,U34	3		
10Kx4 (MUX)	Multiplexor	RN1,RN3,RN4	3		
16MHz	Oscillator	X1,X2,X3,X4	4		
LTC4361-2	overvoltage/overcurrent protection controller safeguards	U2,U5,U8,U10,U15,U37,U38,	9		
SN74LVC2G32	Positive-OR gate	U48,U49	2		
SSM6K514NU	Power Management Switches	Q1,Q3,Q5,Q7,Q8,Q10,Q11,	11		
F100	RESISTOR	R6,R13,R20,R33,R43	5		
F1.0	RESISTOR	R100,R167	2		
F576K	RESISTOR	R105,R113	2		
15k	RESISTOR	R103,R111	2		
F1.07M	RESISTOR	R9	1		
F1M	RESISTOR	R2,R102,R110	3		
F33.2K	RESISTOR	R104,R112	2		
F0.025 (2012) 1/2W	RESISTOR	R5, R12, R18	3		
F0.025	RESISTOR	R1,R8,R15,R25,R26	5		
F0.05 (1608) 1/3W	RESISTOR	R28,R42,R128,R129	4		
F0.5	RESISTOR	R107,R114	2		
F2.0K	RESISTOR	R34,R44	2		
F0.02	RESISTOR	R36,R39	2		
F180K	RESISTOR	R4	1		
F178K	RESISTOR	R11	1		
0	RESISTOR	R17	1		
F82.5K	RESISTOR	R21	1		
F33.2K	RESISTOR	R104,R112	2		
33	RESISTOR	R160	1		
390	RESISTOR	R173	1		
1k	RESISTOR	R38,R41,R122,R126,R140, R141,R144,R145,R146,R147, R148,R149,R159,R175	14		
F.499K	RESISTOR	R7,R14,R23,R24,R35,R45, R46,R47	8		
100K	RESISTOR	R22,R55,R56,R57,R87,R88, R89,R90,R91,R92,R93,R94, R99,R106,R116,R117,R119, R120,R131,R132,R163,R164	22		
4.7uF	RESISTOR	C86,C94,C95,C122	4		
10K	RESISTOR	R3,R10,R16,R27,R40,R48, R72,R101,R108,R109,R115, R123,R124,R125,R143,R150, R151,R152,R153,R154,R155, R156,R157,R158,R161,R162, R168,R176	28		
100	RESISTOR	R29,R58,R62,R64,R65,R66, R67,R68,R69,R70,R73,R74, R75,R76,R77,R81,R82,R83, R84,R86,R95,R96,R97,R98, R118,R121,R127,R133,R134, R135,R138,R139,R142,R165, R169,R171,R177,R178,R179, R180	40		
SN74LVC1G125	Single Bus Buffer Gate With 3-State Output	U47,U54	2		
PIC16F1789-I/PT	START PIC (40 Pin)	U14	1		
STWD100	Watchdog timer circuit	U18,U55	2		

Updated document can be found here

Appendix A

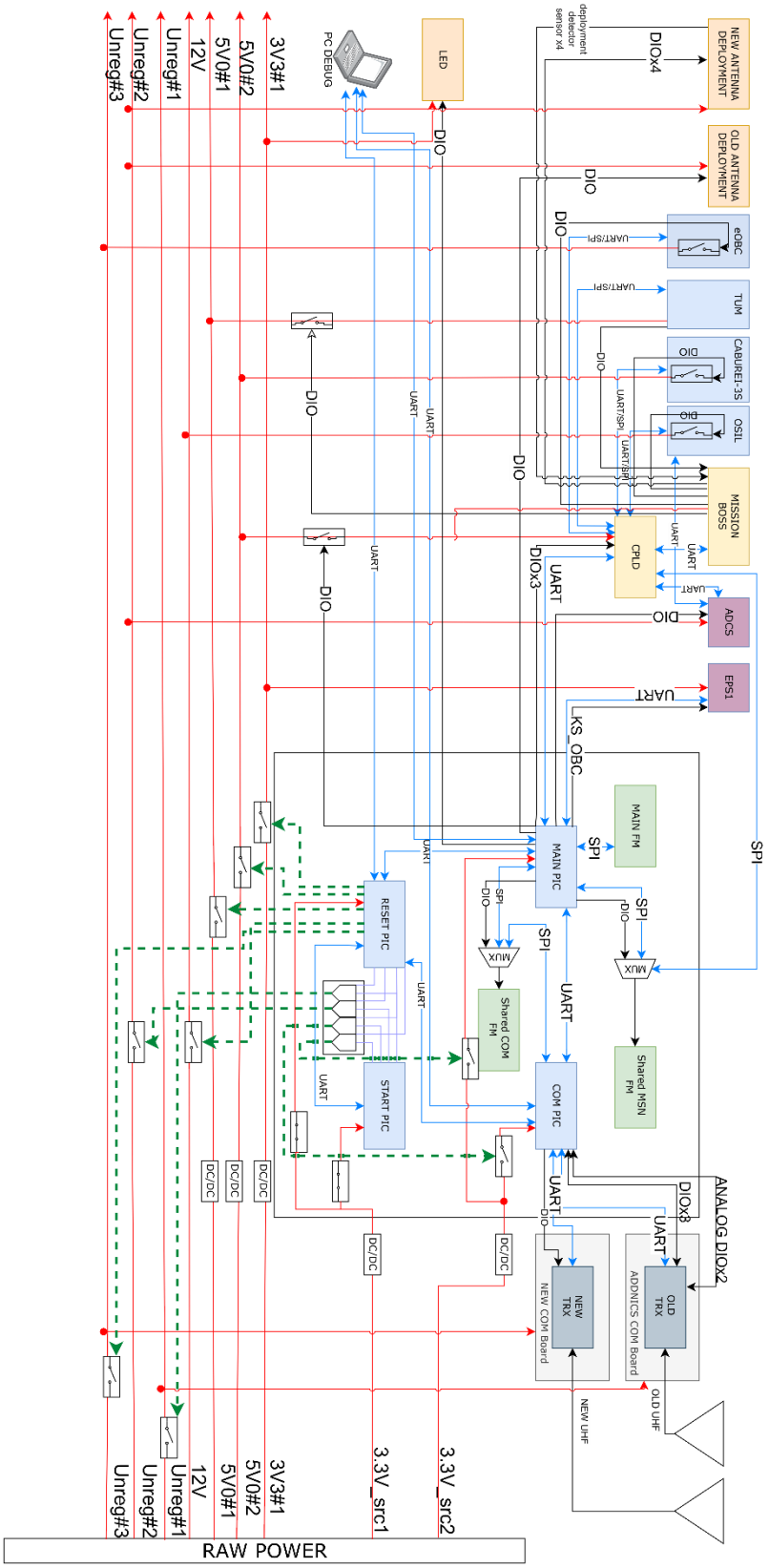


Figure 7-2 Detailed OBC-CDH Block Diagram

Appendix B

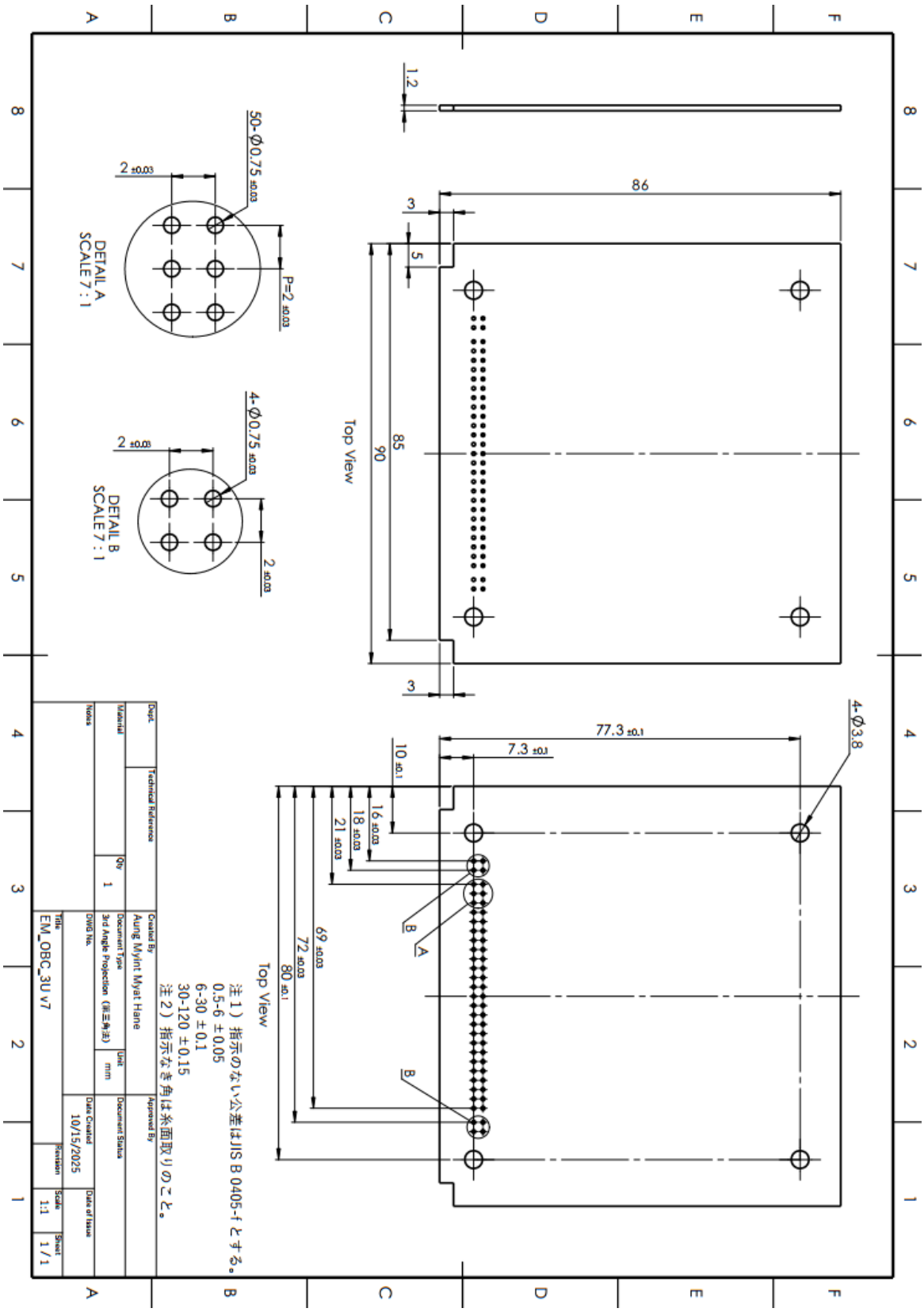


Figure 7-3 OBC/EPS Board 2D drawing